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Performance Study of 13.56 Mhz Full-Bridge Inverter on Wireless Power Transfer System for Electric Vehicle Charging

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Abstract

This research developed a series of GaN MOSFET-based full bridge inverters (TP90H050) with UCC27524 drivers for Wireless Power Transfer (WPT) applications of military vehicles, which are targeted to operate at the ISM frequency of 13.56 MHz. The LTspice simulation showed a potential for near-sinusoidal waves (THD<1%) and a power efficiency of ≈2.13 kW at 50Ω. However, the PCB prototype was only capable of stable operation up to 666.66 kHz with a clean box wave output, and separate tests on fourth-order LC–Butterworth filters achieved a sinusoidal signal with an efficiency of ≈75%. Failure analysis attributed MOSFET damage to switching path length, parasitic effects, and protection limitations. Significant differences were found between the simulation and the implementation at 666.66 kHz, where the hardware RMS voltage was only ≈33% of the simulation. Improvements going forward include the use of precision oscillators/DDSs, drivers with protective features (UVLO and active Miller-clamp), calibrated snubber, and closed controls.

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INTRODUCTION

The defense sector's dependence on fossil fuels remains a serious challenge to global decarbonization efforts, including in Southeast Asia. In Indonesia, increasing fossil fuel consumption is exacerbating the burden on limited energy infrastructure (Müller et al., 2024). Emissions from combat vehicles and other key weapon systems contribute to

worsening air quality, driving a clean energy transition through the electrification of military vehicles (Jamaludin et al., 2021).

The military electric vehicle market is projected to grow rapidly from US$4.1 billion in 2023 to US$20.4 billion in 2030, at a CAGR of 25.6% (MarketsandMarkets, 2024). In Indonesia, the development of electric vehicles such as the Evhero Sergap Senyap by ITENAS (Wardana, 2020) and the Morino EV manufactured by PT Pindad demonstrate real progress in defense electrification (PT Pindad, 2025).

The charging process is a vital component in the continued operation of electric vehicles, both in the civilian and military sectors. Generally, charging is done using a conductive (wired) method, which involves connecting the vehicle directly to a power source using a cable. This method offers high efficiency, ranging from 90–95%, but has drawbacks in terms of flexibility and durability, especially when used in extreme environments.

As an alternative, Wireless Power Transfer (WPT) is gaining traction because it reduces reliance on physical connectors, minimizes the risk of electrical sparks, and supports dynamic charging scenarios while the vehicle is in motion. Various studies have shown that with the right compensation topology design, such as Series-Series (SS) or Inductor-Capacitor-Capacitor (LCC), combined with the use of high-performance materials such as High-Temperature Superconductors (HTS), WPT systems can achieve efficiency levels of up to 95%, comparable to wired methods under optimal conditions. One concrete example of this is the Oak Ridge National Laboratory (ORNL)'s test on an electric Toyota RAV4, which achieved 95% efficiency at a distance of 16 cm (Machura & Li, 2019).

Plug-in charging systems have several limitations, particularly in military operations. This method requires the vehicle to stop and physically connect to a power source, which reduces mobility and is susceptible to damage from extreme environmental conditions such as dust and harsh weather. Alternatively, Wireless Power Transfer (WPT) technology enables contactless wireless charging, increasing the flexibility and reliability of military operations (Pooja Mangraiya & Brijendra Mishra, 2023).

For WPT to operate optimally, a GaN MOSFET-based Full-Bridge Inverter capable of operating at an ISM frequency of 13.56 MHz is required. This type of inverter offers high power conversion efficiency, stable waveforms, and a more compact size thanks to its high switching frequency. Furthermore, the fast switching characteristics of GaN MOSFETs generate less heat, reducing cooling requirements, and improving response to load changes. This combination enables WPT to operate efficiently and reliably in demanding military environments (Sulistyo et al., 2023).

Therefore, the researchers submitted a study entitled "Performance Study of a 13.56 MHz Full-Bridge Inverter in a Wireless Power Transfer System for Electric Vehicle Charging."

Literature Review

Full-Bridge Inverter

Power inverters are a key element in Wireless Power Transfer (WPT) systems, especially in electric vehicle wireless charging applications. This component converts direct current (DC) into alternating current (AC) at a certain frequency to produce resonance conditions between the transmitting unit and the receiver. This resonance plays an important role in minimizing power loss and improving energy transfer efficiency. This study, using the frequency 13.56 MHz, which belongs to the ISM (Industrial, Scientific, Medical) band, for capacitive-based high-power WPT applications (Muharam et al., 2020).

GaN MOSFET

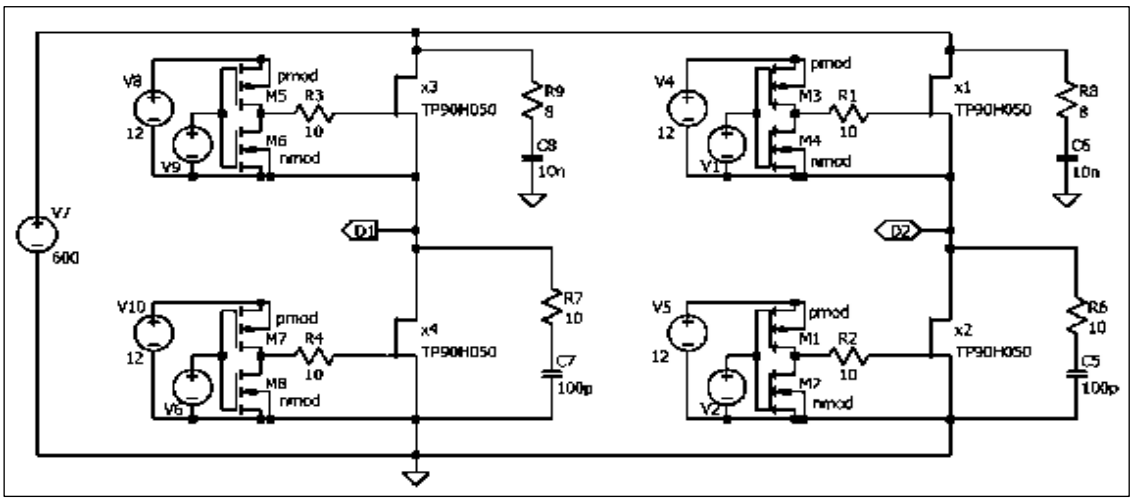


Figure 1. Full-Bridge inverter Network Model

(Source: Sulistyo et al., 2023)

The Gallium Nitride Metal Oxide Semiconductor Field Effect Transistor (GaN MOSFET) is one of the modern semiconductor innovations that has the ability to work at high frequencies with superior efficiency while significantly reducing power losses. (Saltanovs & Krainyukov, 2019).

Table 1. Performance Comparison of MOSFET Types

Property	**Si**	**SiC**	**GaN**
E_G (eV)	1.12	3.2	3.4
E_{BR} (MV/cm)	0.3	3.5	3.3
V_s (x 10^7 cm/s)	1.0	2.0	2.5
μ (cm^2/Vs)	1500	650	990

(Sumber: Xu et al., 2019)

Table 1 compare the main characteristics of several types of MOSFETs, namely GaN, silicon (Si), and silicon carbide (SiC). From the table, it can be seen that GaN, with a band gap of 3.4 eV, supports switching processes at very high frequencies, including the 13.56 MHz commonly used in WPT systems, and remains efficient under high voltage and temperature conditions. In contrast, silicon that only has a band gap of 1.12 eV tends to be more limited in high-frequency and voltage applications. As such, GaN stands out as the best choice for high-power applications that require fast switching and high efficiency.

Dead-time Generator

Dead-time is a method used in a full-bridge inverter circuit to provide a time lag between the high-side and low-side MOSFETs switching process, as shown in Figure 2.6. The main function of this pause is to avoid short circuit conditions due to both switches being active at the same time, which has the potential to damage the MOSFET. Dead-time settings can be done both through hardware and through software on a microcontroller (Sulistyo et al., 2023).

The similarities include:

Table 2. MOSFETS equation

$T = \frac{1}{f}$
$SW_{time} = 6$ ns
$T_{dt} = 10\% \times T$, atau
$T_{on\_hi} = \frac{T}{2} - SW_{time} - T_{dt}$
$T_{on\_low} = \frac{T}{2} - SW_{time} - T_{dt}$

Impedance Matching

Appropriate impedance is essential to ensure that the transfer of power from the inverter to the load takes place efficiently. Impedance matching is usually achieved by

adding an inductor (L) and a capacitor-based compensation network (C), which can be assembled in a series, parallel, or a combination of the two configurations (M. Zhang et al., 2020).
The similarities include:

Table 3. Impedance Matching

$\overrightarrow{X_L} = j\omega \times L$
$\overrightarrow{X_c} = \frac{1}{j\omega \times C}$
$Q = \frac{\overrightarrow{X_L}}{R_L} = \frac{\overrightarrow{X_c}}{R_L}$
$L = \frac{Q \times R}{j\omega}$
$C = \frac{1}{(j\omega \times R \times Q)}$

RESEARCH METHODS

This research uses a quantitative approach, which aims to produce measurable numerical data to be analyzed objectively. The main focus of the research is on the design, simulation, and implementation of GaN MOSFET-based Full-Bridge Inverter in Wireless Power Transfer (WPT) systems. The initial stage was carried out by simulation using LTspice software, then the results were validated through physical experiment testing. The research process also follows the waterfall model, which is a development method that is systematically arranged.

Research Design

This research design combines simulation design and experimental design which begins with the observation stage. The researcher used mathematical models and hardware simulations to obtain supporting data in testing hypotheses regarding the efficiency and quality of power transfer. The waterfall model was chosen to guide the sequence of research stages from design, implementation, to testing, as shown in Figure 2.

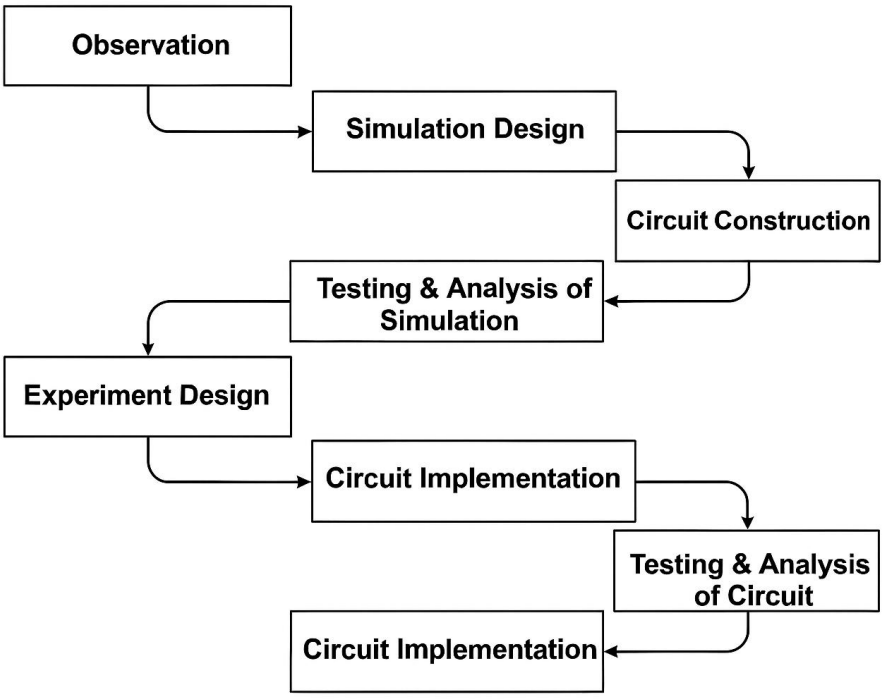


Figure 2. Waterfall Model Diagram Research Design

Tool Needs Analysis

In the performance study of the 13.56 MHz full-bridge inverter in the wireless power transfer system for electric vehicle charging, some of the tools and materials used to realize it include:

Table 4. Research Tools and Materials

Tool	Material
Desktop Intel Core i7-9750H ; RAM: 16 GB	Gate drivers UCC27524
LTspice	TP90H050 GaN MOSFET
PSoC Creator 4.4	IC Isolator SI8641
Easy EDA	IC NAND 74HC10
Power Supply Unit	IC Schmitt Trigger 74HC14
Hantek 6000 Series	DC-Isolated Supplys
Digital Multimeter	CY8CKIT-059 PSoC® 5LP Ki
	Capacitors
	Inductors
	Resistors
	Printed Circuit Board (PCB)
	PCB Terminals
	Soldering Materials

Research Procedure

System workflow in Figure 3 The process starts from the input DC source, which comes from the rectifier or other external DC source. Furthermore, a Pulse Width Modulation (PWM) signal is generated by the microcontroller to regulate frequency, duty cycle, and dead-time, so that the activation of the upper and lower side MOSFETs is maintained.

After PWM configuration, this signal is passed to the GaN MOSFET to perform power switching according to a predetermined pattern. The system then checks whether the frequency of 13.56 MHz has been reached. If achieved, the process is continued to the switching stage at that frequency; if not, then the PWM signal is readjusted.

The output from the MOSFET in the form of an AC signal is then passed to the LC Filter to reduce the harmonics, so that only the main frequency is retained. In the next stage, impedance matching is performed to ensure power can be efficiently transferred to the load.

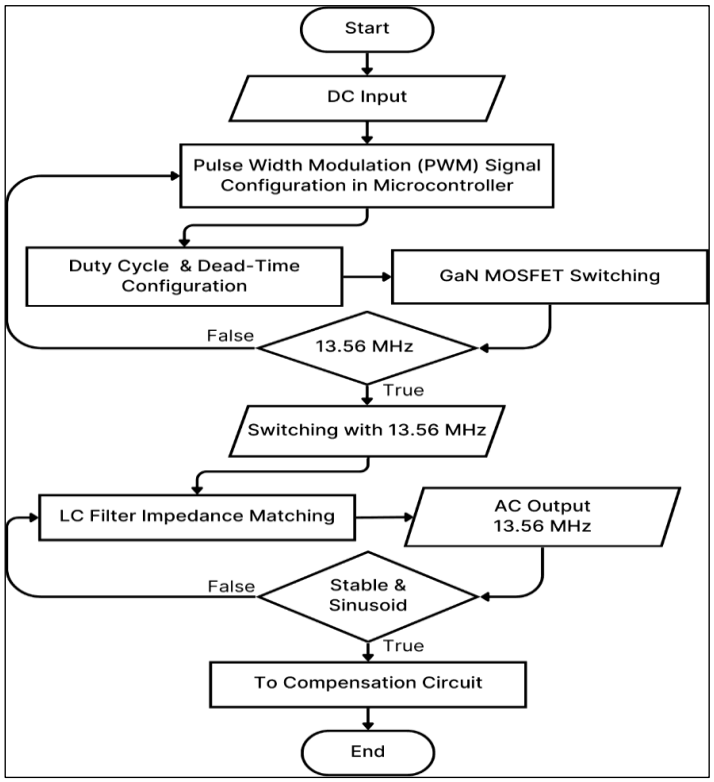


Figure 3. System Workflow Flowchart

The system then verifies the stability of the output signal. If the signal is a stable sinusoidal form, power is routed to the compensation circuit and the primary capacitive plate to be transferred to the electric vehicle.

RESULTS AND DISCUSSION

Simulation Parameter Calculation Results

Based on the equation of tables 1 to 3, the values for the simulation parameters can be searched as follows.

$T = \frac{1}{f} = \frac{1}{13.56 \times 10^6} \approx 73.746$ ns

$SW_{time} = 6$ ns

$T_{dead\_time} = 10\% \times T = 7.374$ ns

$T_{on\_hi} = \frac{73.746}{2} - 6 - 7.374 = 23.499$ ns

$T_{on\_low} = \frac{73.746}{2} - 6 - 7.374 = 23.499$ ns

LC Low-Pass Filter Calculation Results

Based on Butt Filter TheoryBased on the Butterworth Filter theory, if 4 components are used with a configuration starting from capacitor (C), then the filter is of the 4th order with the order of components from L1 to C4. The value of the quality factor (Q) obtained was Q1 = 0.76537 and Q2 = 1.84776. Using equations (2.7) to (2.13), as well as the parameters RL = 50 Ω and R = 1/2 RL = 25 Ω,, the filter value of each component L and C can be searched as follows:

$R_L = 50\ \Omega$, $R = \frac{1}{2} R_L = 25\Omega$

Maka:

$L1 = \frac{Q \times R}{j\omega} = \frac{Q1 \times R}{2 \times \Pi \times f} \approx 0.225\ \mu H$

$C2 = \frac{Q \times R}{(j\omega \times r \times Q1)} \approx 0.613$ nF

$L3 = \frac{Q \times R}{j\omega} = \frac{Q2 \times R}{2 \times \Pi \times f} \approx 0.254$ nF

$C4 = \frac{1}{(j\omega \times R \times Q2)} \approx 0.254$ nF

Simulation Design Results

Based on the calculations in the previous chapter, the inverter design was then modeled and tested using LTspice software. The main parameters used include a switching frequency of 13.56 MHz, a dead-time value of 10% of the period, and a switching time (SW_time) of 6 ns. The Time on High (ON_H) and Time on Low (ON_L) values are obtained by subtracting the SW_time and dead-time from half the signal period.

For signal quality analysis, Total Harmonic Distortion (THD) is calculated via Fourier transform at a frequency of 13.56 MHz. The time step range is set between 1 µs to 1.5 µs so that only signal samples in stable conditions are analyzed.

```
.tran 0 5u 1u
.meas TRAN Vm MAX V(n010,n011)
.meas TRAN Vpp PP V(n010,n011)
.meas TRAN Vrms RMS V(n010,n011)
.meas TRAN Pavg AVG V(n010,n011)*I(RL)
.four 13.56meg I(RL)
.param Vin=9
.param Rg=3.3
.param L1=0.224µ
.param C2=0.613n
.param L3=0.542µ
.param C4=0.254n
.param Fsw=13.56meg
.param SW_time=6n
.param Psw=1/{Fsw}
.param dead_time={{Psw}*0.1}
.param ON={{Psw}/2-{dead_time}-{SW_time}}
.param delay= {{Psw}/2}
```

Figure 4. Ltspice Simulation Parameters

Figure 4 shows the LTspice simulation parameters set via the .param command, including variables such as Vin, T, SW_time, and dead_time. Adjusting these parameters ensures that the gate driver pulses are generated alternately without overlap, while maintaining dead-time so that switching losses can be minimized. Thus, this design emphasizes the importance of precise switching control at the simulation level.

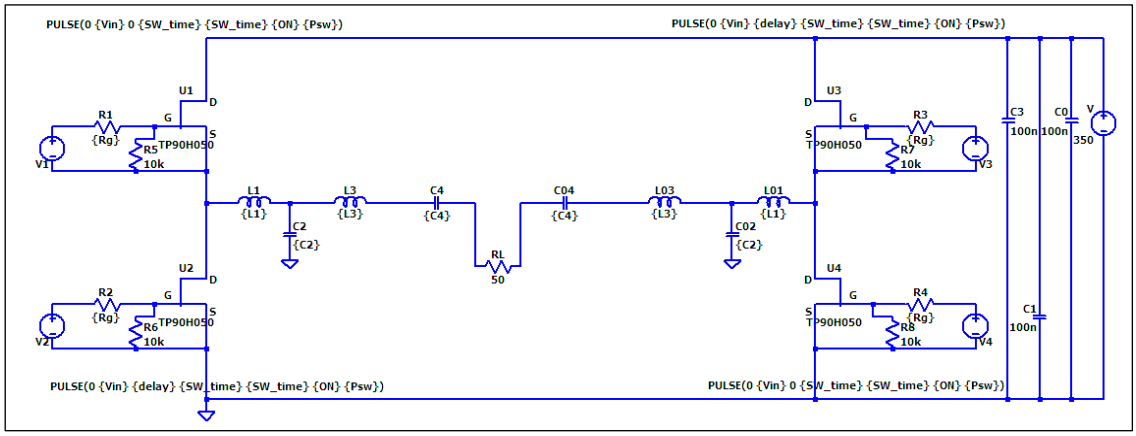


Figure 5. Desain Rangkaian Simulasi Ltspice

Figure 5 shows the complete schematic of the simulation circuit, consisting of the input source (Vin), main and complementary MOSFETs, driver circuits, and LC Low-Pass Filters on the output side. This series aims to evaluate the performance of inverters at a frequency of 13.56 MHz, especially in regulating output voltage, load current, transient response, and ripple voltage. The results of the simulation are expected to provide initial verification of the theoretical calculations that have been carried out. Thus, this simulation serves as an important reference before the real implementation of hardware.

Simulation Experiment Results

Simulation testing was performed with DC input voltage variations from 50 V to 325 V, using a resistive load of 50 Ω. The results are shown in Figure 4.3, where the inverter output is in the form of a sinusoidal AC wave, while the switching signal of the MOSFET before passing through the filter still appears to be in the form of a square wave. This confirms the role of the filter in producing the signal quality according to the specifications in the upper part of Figure 5, the output of the LC filter already shows a pure sinusoidal shape. The middle section depicts the power flow in the circuit, while figure 6 and 7 summarizes the data from the simulation results with the input voltage variation. This information is important to observe the relationship between the DC input and the output quality of the inverter.

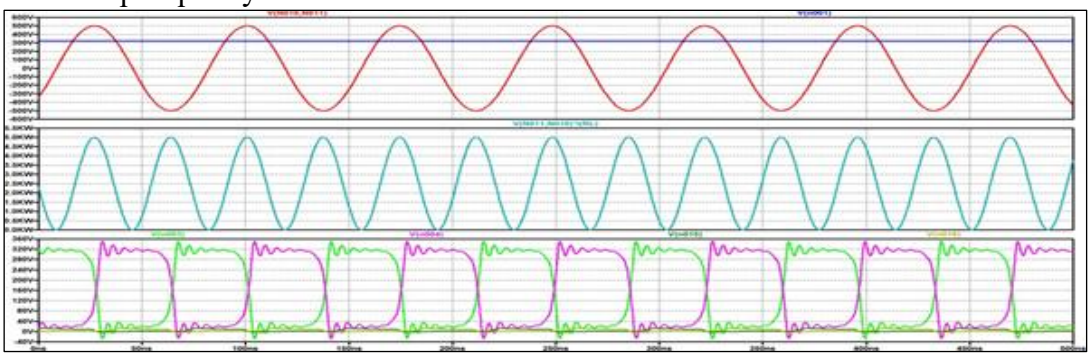


Figure 6. Ltspice Simulation Series Design

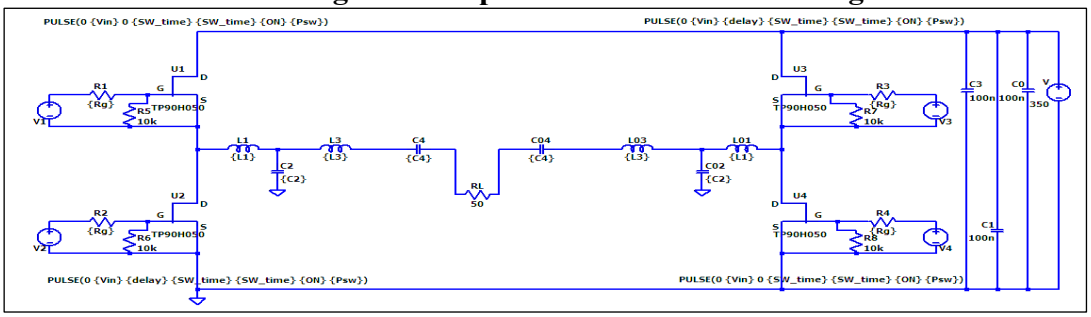


Figure 7. 325V Simulation Results

From the figure, it can be seen that the increase in input voltage (Vin) results in a proportional increase in RMS voltage (VRMS) on the AC output side. This has an impact on the increase in average power (PAVG). In addition, a low THD value (0.45–1.00%)

indicates that the output signal quality is close to the ideal sinusoidal, so the DC–AC conversion process can be said to be efficient. Thus, the performance of the inverter at the simulation level is proven to support the high efficiency target.

Microcontroller Setting Results

Microcontroller setup is done using PSoC Creator 4.4 software. In the initial stage, the clock system configuration is set as shown in table 5. The system's master clock is adjusted to be close to four times the inverter's target frequency, which is 54.24 MHz (≈ 4 × 13.56 MHz). This step is an important foundation for the stability of PWM signals at high frequencies.This process includes selecting the clock source, adjusting the Phase Locked Loop (PLL), and adjusting the divider so that the frequencies produced are suitable for PWM operation. This arrangement is essential so that the PWM signal used in MOSFET control is of high precision and in sync with the planned switching frequency.

Table 5. Full-Bridge Inverter Simulation Output Table

No	VIN	VM	VPP	VRMS	PAVG	THD
	[V]	[V]	[V]	[V]	[W]	[%]
1.	50	62,040	124,262	43,692	59,151	0,521
2.	75	101,451	202,432	70,961	100,732	0,600
3.	100	139,222	278,841	98,050	192,26	0,631
4.	125	177,596	355,282	125,981	317,400	0,622
5.	150	217,354	434,658	154,160	475,292	0,622
6.	175	256,803	513,589	182,222	664,122	0,622
7.	200	295,851	591,740	210,323	884,721	0,622
8.	225	335,589	671,191	238,564	1138,234	0,622
9.	250	360,191	718,152	252,644	1276,489	0,541
10.	275	389,832	780,123	276,121	1524,817	0,489
11.	300	424,741	849,058	299,785	1797,413	0,450
12.	325	479,303	960,310	326,978	2138,281	1,001

Furthermore, the results of PWM output measurements in Figure 8 show that the signal produced is at a frequency of about 13.51–13.59 MHz, according to the target. The waves measured on the oscilloscope are generally square, although at high frequencies there may be slight distortion due to parasitic factors and the setup of measurements using jumpers. A small difference between the measurement frequency and the target frequency is still acceptable, given the component tolerance and the limitations of the internal clock precision.

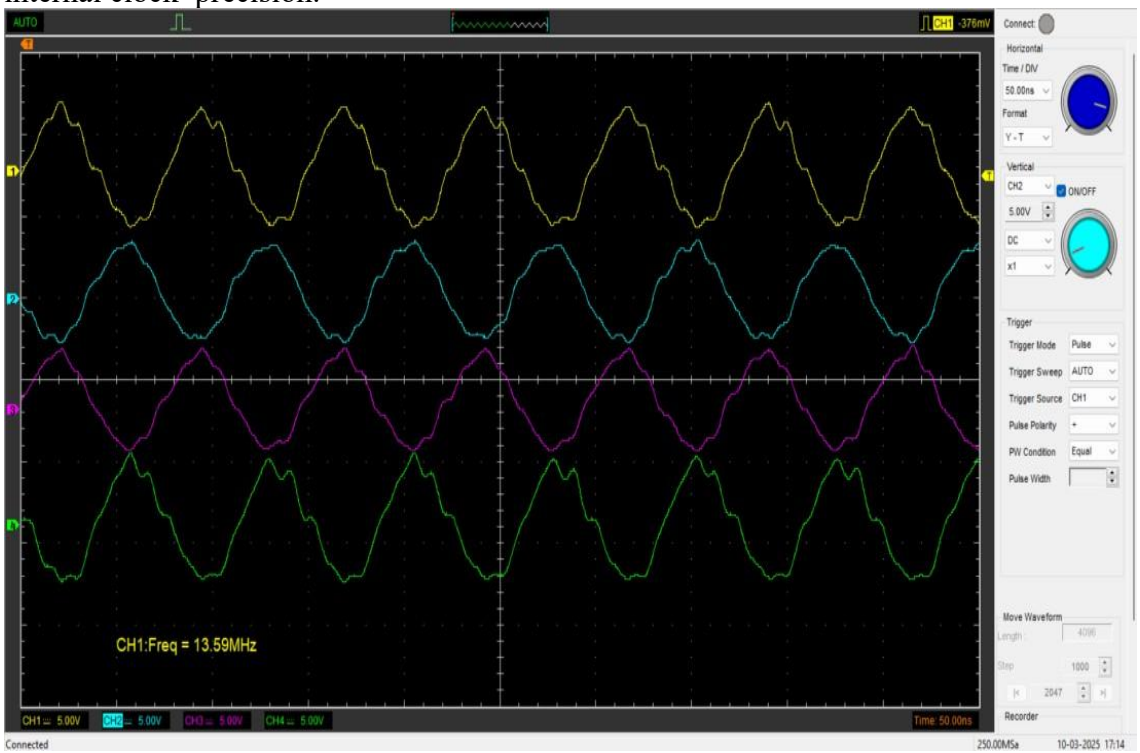


Figure 8. PSoC 5 LP PWM Output Measurement Results

Dead-time Setting Results

The dead-time setting this time is set using hardware with a scheme of input signals entering the NAND IC 74HC10 and then the output is fed into the Schmitth Trigger IC 74HC14 so that the signal is non-inverting again and corrects the input signal to a box. Where the RC delay circuit is arranged with a resistor connected to a capacitor that is paralleled to the ground, where the delay time is calculated in Equation 2.4, namely:
If the value is set C=100pFF, then:

$$R==104.95\Omega\approx100\Omega\frac{10\%\ X\ Period}{100_p\ X\ 0.7}$$

In this design, a dead-time of 7,347 ns is set, so that a resistor close to 104.95Ω is obtained, namely a 100Ω resistor.

Schematic Design and PCB Layout Results

The schematic design and layout of the PCB carried out using the EasyEDA Pro software can be seen in Figure 9. The first schematic of the configuration recommended in the UCC27524 driver gate datasheet, with the placement of capacitors and resistors that function as protection elements against voltage fluctuations and ripples at both inputs and outputs. The system uses an isolated power supply of 3.3V for the signal circuit, and 9V for the gate driver power supply (VDD).

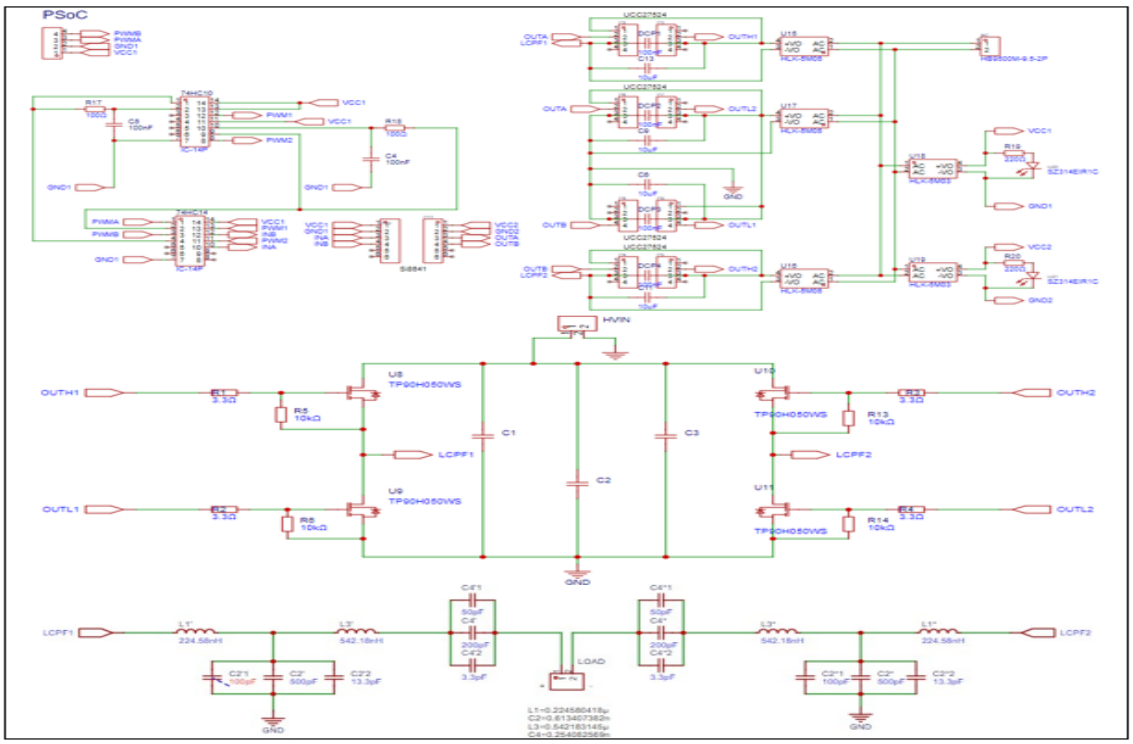


Figure 9. Schematic Control, Switching, and Filter Section Sets

In the MOSFET switching system, four gate drivers are used UCC27524 to control the four GaNFET TP90H050, as well as to provide isolation and protection for the PSoC 5 LP microcontroller. Output signals such as OUTH1&2, OUTL1&2, and LCPF1&2 are arranged so that the schematic is divided into three main parts to facilitate the design process.

The second schematic features a Full-Bridge inverter circuit, consisting of four GaNFETs, three protection capacitors, and four resistors. A 3.3Ω resistor is used on the gate path as a current limiter when switching, while a 10kΩ resistor serves as a pull-down to ensure a low logic level when the MOSFET is off. The circuit also includes three terminals: HVIN as the input DC voltage, and two DV terminals as the output from the inverter that has not yet gone through the filtering process.

The schematic of the filter section is adjusted according to the simulation series, namely there are 4 inductors and 4x3 capacitors. The capacitor slot is divided into 3 because no capacitor has the expected capacitance so the capacitors are summed in a parallel manner to get a close result. Then there is the output terminal of this circuit which is expected to produce AC electricity.

PCB design uses a double-layer configuration to accommodate the complexity of the circuit. The top layer is used for small components and control signals, while the bottom layer is reserved for MOSFETs and large current paths, so that the heat generated can be more easily channeled and controlled. The placement of the MOSFETs on the underside of the PCB is also designed to facilitate the installation of the heatsink, as shown in Figure 10.

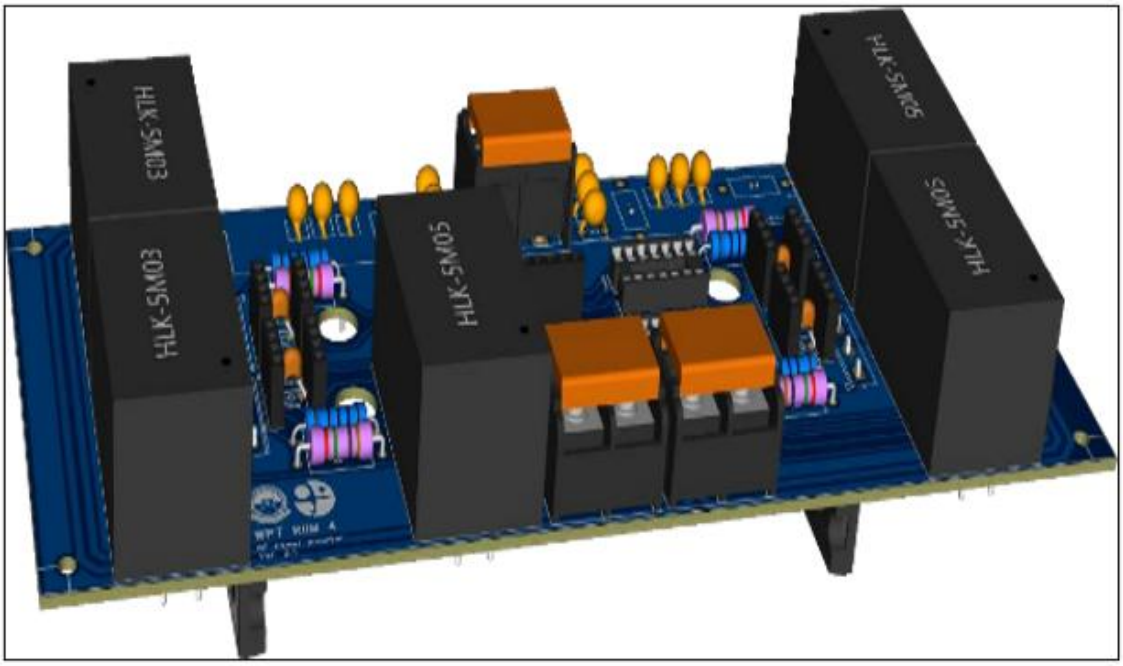


Figure 10. PCB 3D View

In the power supply system, five large AC-DC isolated supply modules are used which function to supply a series of signal generators and each gate driver. There are two input terminals on the front—one for DC voltage to VDD MOSFET and one for AC voltage entering the isolated supply. Meanwhile, the output terminal for the AC signal from the inverter filter is placed on the back of the PCB.

Network Testing Results

Table 6. Series Test Results

Parameter	Status
High DC Inp.	5,08 Volt
Current Inp.	2,91 Ampere
Freq. Input Gate driver	13,59 MHz
Freq. Output Gate driver	13,59 MHz
Freq. Output Full-Bridge	13,81 MHz
Freq. Output Filter	13,51 MHz
Out. VRMS Full-Bridge	3,22 Volt
Out. VRMS Filter	1,09 Volt

Initial testing successfully generated a sinusoidal signal at the AC output when a 5V input was provided as shown in Figure 11.

However, the system experiences significant power loss and high input current (reaching 2.90 A), close to the maximum limit of a DC Generator. This condition indicates an anomaly in the full-bridge inverter circuit, so a thorough evaluation of each subsystem is required to identify the source of the fault, as shown in Table 6.

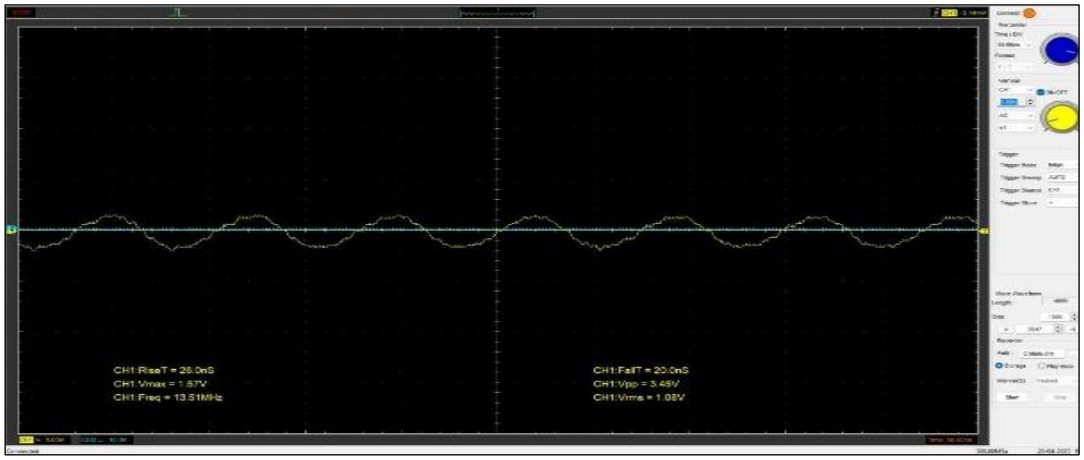


Figure 11. AC Frequency Output

PWM Review Results & Frequency

The re-evaluation stage is carried out by checking the PWM configuration as well as the frequency of inverter operation as shown in figure 12. The results of oscilloscope observations showed that at a frequency of 13.56 MHz, the output signal was still filled with ringing and considerable noise. This condition causes cross-conduction between the top and bottom side MOSFETs, thereby triggering circuit instability and the risk of component damage.

To solve this problem, a test is carried out by lowering the switching frequency as shown in the same table. A decrease in frequency results in improvements in the PWM signal form: the waves look cleaner, clear box, and the maximum voltage becomes higher. However, this change in frequency also has implications for the dead-time that was previously set for high-frequency operations.

The dead-time designed for the 13.56 MHz frequency is too narrow when applied at low frequencies, resulting in the output of the gate driver being suboptimal, even increasing the risk of shoot-through or signal overlap, as noted in figure 12. To adjust to these conditions, the value of the resistor in the dead-time circuit is changed to 1 kΩ, while the capacitor is maintained at 100 pF. The test results showed that this new combination provided a dead-time of about 70 ns at 666.66 kHz, which was then re-verified through gate driver output signal measurements.

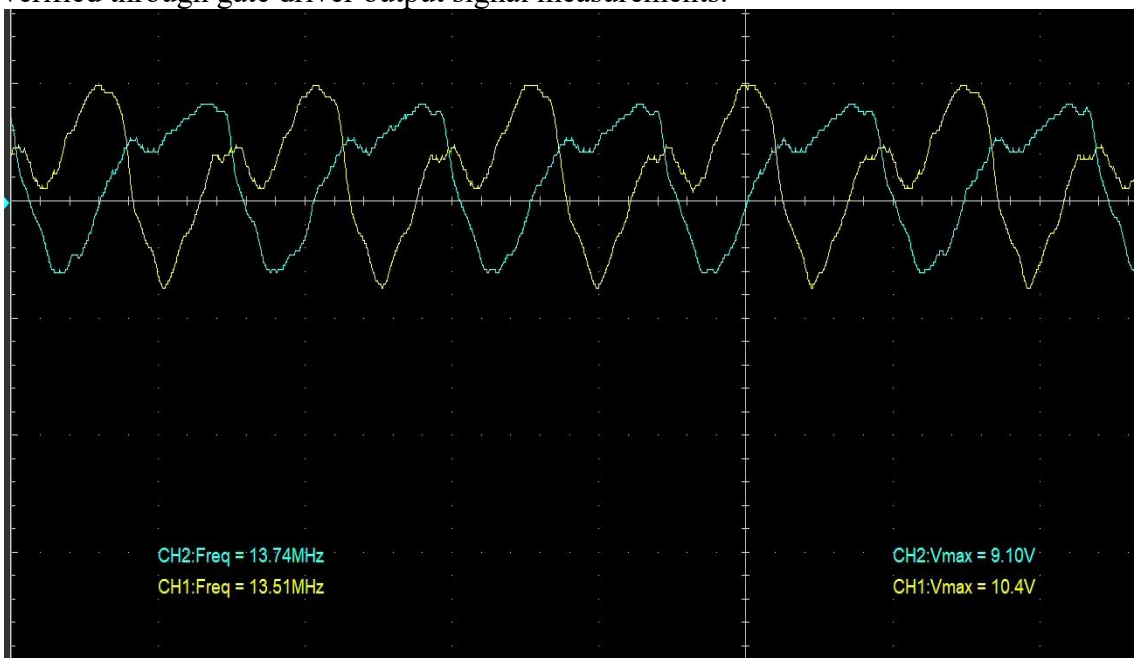


Figure 12. PWM, Frequency, and Dead-time Review Results

R=1KΩ and C=100pF Adjustments for Lower Frequencies

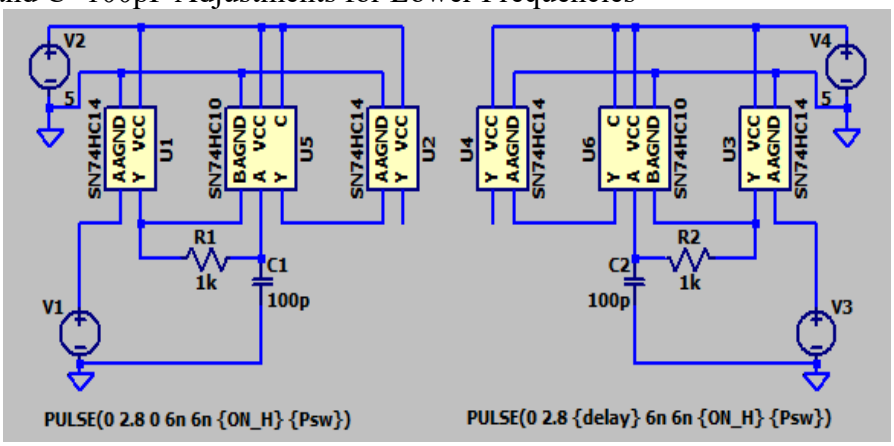
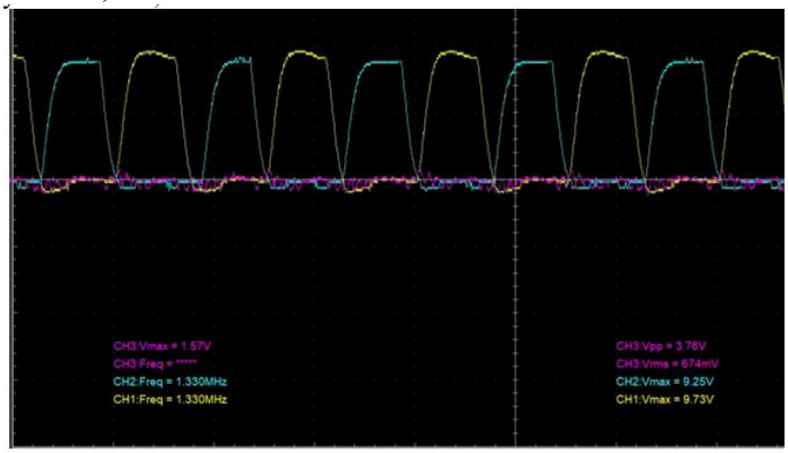


Figure 13. PWM, Frequency, and Dead-time Review Results

The output of the gate driver is suboptimal and is often read by the oscilloscope Frequency ±1.33 MHz, with a Dead-time of 15.4ns



Fsw = 666.66 kHz, R = 1KΩ and C = 100pF (DT=70ns)

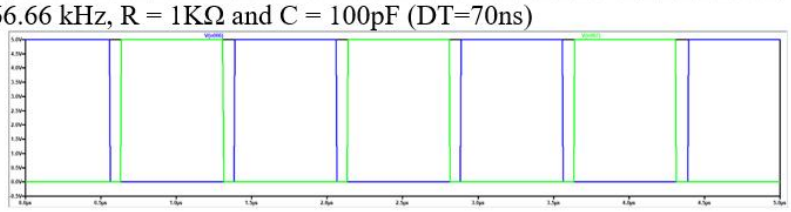
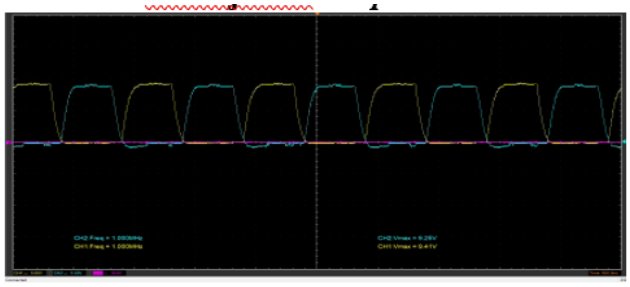
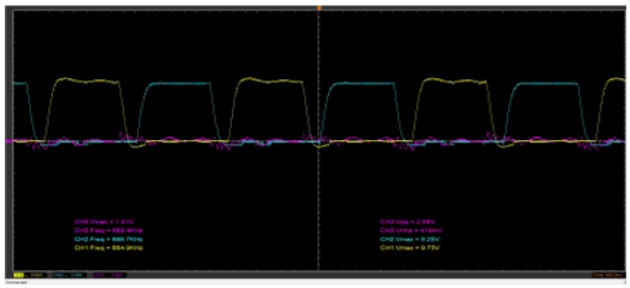


Figure 14. Fsw = 666.66 kHz, R = 1KΩ and C = 100pF (DT=70ns)

Gate driver Review Results



Frequency 1 MHz, DT=15.4ns.



Frequency 666.66 kHz, DT=70ns.

Figure 15. Output Gate Driver Review Results UCC27524

Table 7. MOSFET Condition Check Results

MOSFET	D-S (Ω)	G-S (Ω)	Ket.
High-left	2	10	Short
High-right	3	31	Short
Low-left	4	80	Short
Low-right	7	67	Short

After a dead-time evaluation, the output on the gate driver needs to be proven on the circuit. It can be seen in Table 7, where by adjusting the dead-time, the on/off time range is safer than before adjusting.

MOSFET Review Results

An evaluation was also carried out on the condition of the MOSFET TP90H050 after the occurrence of cross-conduction. Resistance checks are performed between the drain-source (D-S) and gate-source (G-S) terminals, with the criterion that the MOSFET is declared to be good if all resistances exceed 500 Ω. On the other hand, if the resistance is below 20 Ω or produces a "beep" sound on the multimeter, then the component is considered damaged.

The test results summarized in Table 4.5 show that the four MOSFETs have been damaged (short) on both the high and low sides. In addition to the cross-conduction cause, this damage is also suspected to be influenced by the limitations of measuring instruments, especially the Hantek 6000 series oscilloscope which uses common ground. This causes the high-side and low-side terminals to share the same ground when measured, thus triggering a short circuit.

Full-Bridge Inverter Review Results

After all the adjustments were made, the full-bridge inverter test continued at the frequency that had been lowered, which was 666.66 kHz. Filters were not used in this test, as the pre-designed filter was indeed intended for the frequency of 13.56 MHz. The test was conducted using a 50 Ω resistive load with different variations of High-Voltage DC (HDC) inputs, and the results are shown in figure 16.

From the test results, it can still be seen that there is ringing in the inverter output, even larger when the input voltage is increased. This interferes with the accuracy of the output frequency readings even though switching frequency decreases and dead-time adjustments have been made.

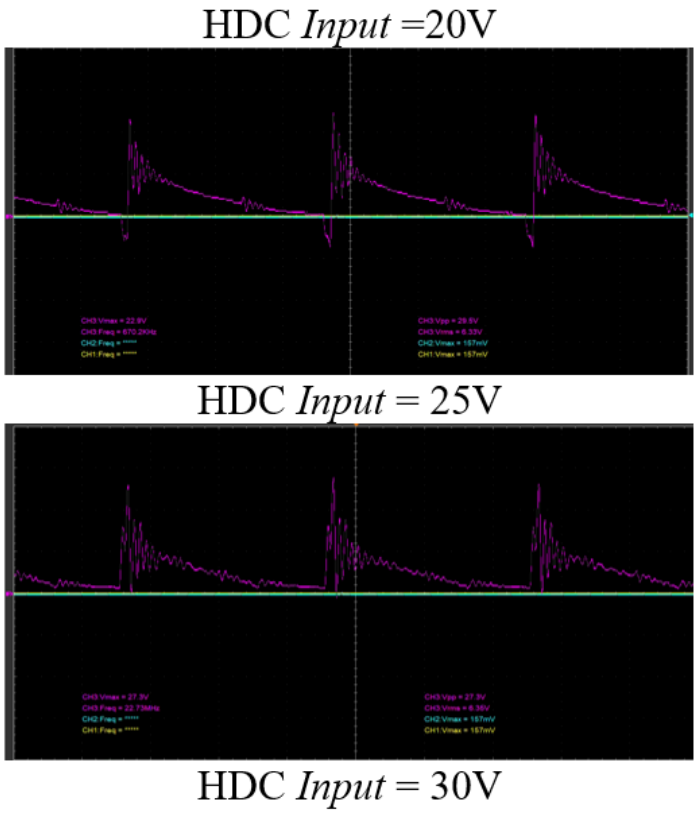


Figure 16. Test Results with Frequency 666.66kHz

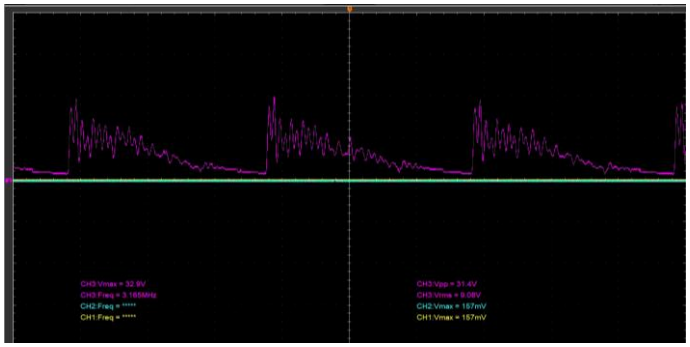


Figure 17. Test Results with Frequency 666.66kHz

To obtain an equivalent comparison, simulations were also carried out at the frequency of 666.66 kHz, the results of which can be seen in figure 17. This comparison shows that the real implementation results are still much different from the simulation results, especially in terms of RMS voltage and power efficiency.

Band Pass Filter Review Results

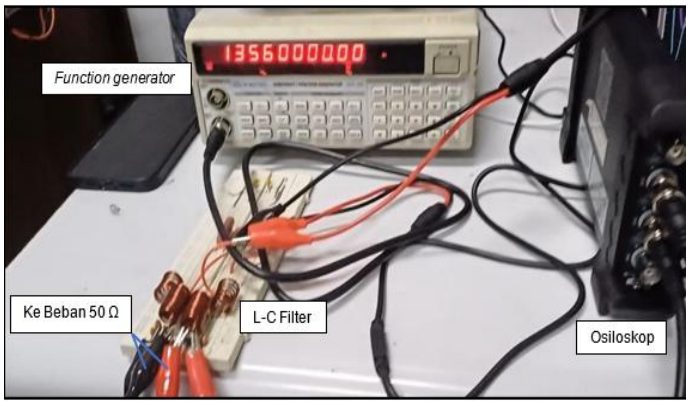


Figure 18. Band Pass Filter Testing

The final evaluation focused on the band-pass filter tested using a function generator with a maximum amplitude of 10 V. Tests were carried out on the breadboard as shown in Figure 3.15, with frequency variations of 1 MHz and 13.56 MHz both under no load and with a load of 50 Ω. The results are presented in figure 18.

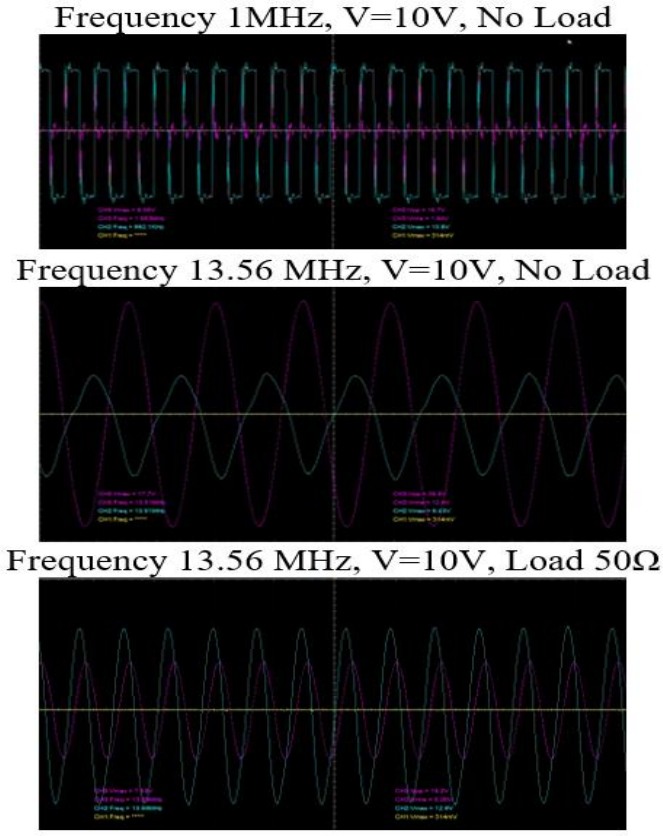


Figure 19. Band Pass Filter Test Results

Table 8. Test Results with Frequency 666.66kHz

V_{IN}	Simulation			Implementation		
	V_M	V_{PP}	V_{RMS}	V_M	V_{PP}	V_{RMS}
	[V]					
5	7,3	14,6	4,8	6,1	12,5	1,3
10	11,9	23,8	9,4	10,4	18,4	3,1
15	16,3	32,6	13,9	16,3	21,0	4,9
20	21,3	42,6	18,5	22,9	29,5	6,3
25	27,8	55,5	23,0	27,3	27,3	6,4
30	33,1	66,3	27,6	32,9	31,4	9,1

From the tests, it was seen that although the filter is capable of working at a wide range of frequencies, the ringing phenomenon still appears when the frequency gets higher. However, as it approaches the target frequency of 13.56 MHz, the sinusoidal signal shape in the filter output becomes clearer with greater amplitude. When a 50 Ω load is used, the amplitude decreases from 10 V to about 7.53 V, which means the filter efficiency is in the range of 75.3%.

Thus, although the filter has shown quite good performance, optimization is still needed to be used effectively in high-frequency inverter systems.

Discussion of Full-Bridge Inverter Series Simulation Performance

The simulation results on LTspice show that the GaN-based Full-Bridge Inverter series of MOSFETs is capable of producing stable and near-sine AC voltages at a frequency of 13.56 MHz. The comparison graph between the input voltage DC (VIN) and the output voltage RMS (VRMS) in Figure 5.1 shows a linear relationship: the higher the VIN, the higher the VRMS, the higher the VRMS, reflecting efficient DC-AC power conversion.

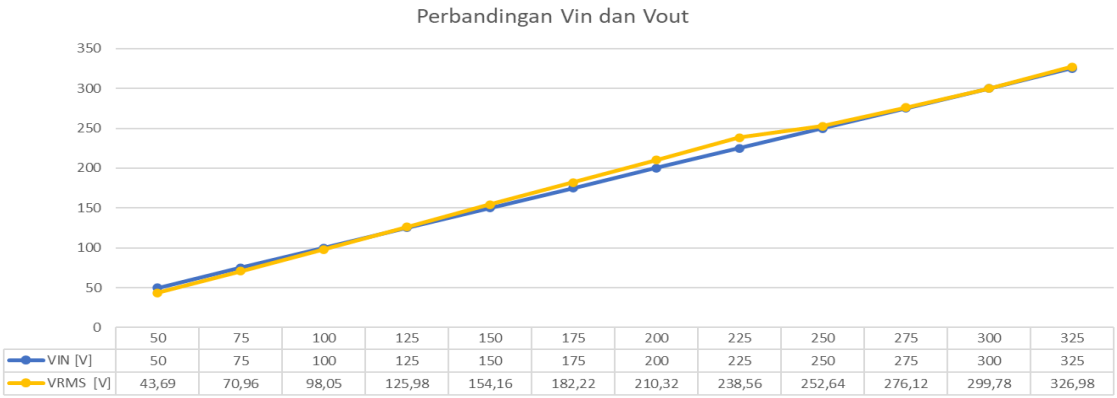


Figure 20. Vin and Vout Comparison Chart

Furthermore, Figure 20 shows that the average power (PAVG) also increases as the VIN increases, which indicates the capacity of the inverter to transfer more power to the load. The wave quality was also confirmed to be very good with an average Total Harmonic Distortion (THD) of 0.61%, and only rose to ±1% when the VIN > 300 V (Figure 21).

This shows that the inverter at the simulation level is capable of providing optimal performance in a Wireless Power Transfer (WPT) system.

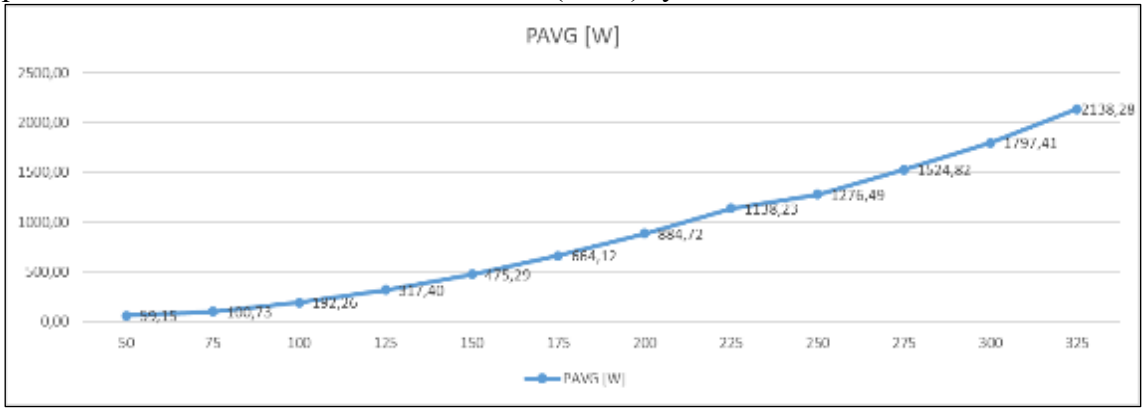


Figure 21. Vin and Vout Comparison Chart

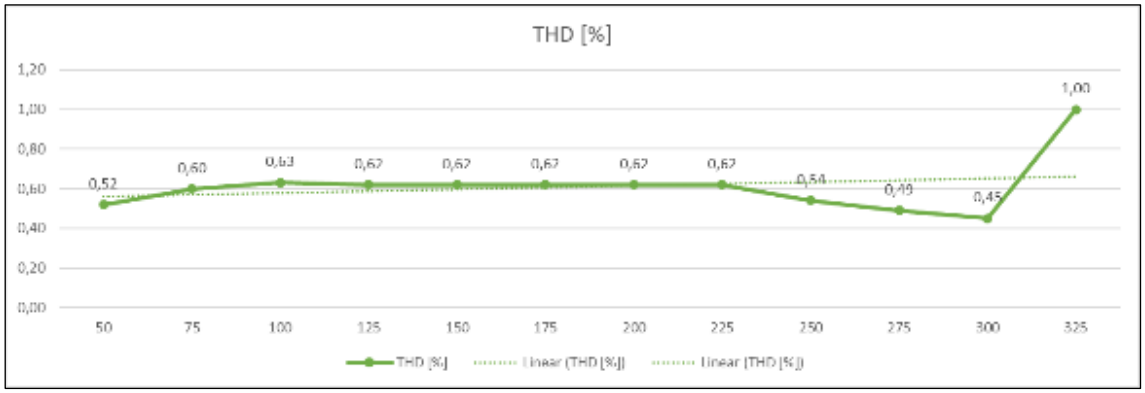


Figure 22. THD Chart

Discussion of the Performance of the Implementation of the Full-Bridge Inverter Series

Physical implementation testing shows different results from simulations. Figure 22 summarizes the results of the review of each subsystem. From the results of the subsystem evaluation, the performance of the new implementation is optimal at frequencies well below the target and requires dead-time parameter tuning, additional protection, and PCB layout optimization to achieve stability and signal quality at 13.56 MHz.

Discussion of Simulation and Implementation Comparison

To fairly compare performance, additional simulations were performed at 666.66 kHz, the highest stable frequency achieved by the physical prototype. The results in table 9 show that although the peak voltage trend increases with the VIN, the implementation VRMS value only reaches 32.9% of the simulation (9.08 V vs. 27.57 V at 30 V VIN), signifying much lower efficiency.

Table 9. Summary of Evaluation of Full-Bridge Inverter Implementation Subsystems

Subsistem	Key Results	Conclusion
PWM & Frekuensi	The PWM signal is stable at only 666.66 kHz; lots of ringing and cross-conduction at 13.56 MHz	Not yet stable at the target frequency; Need for a high-frequency custom driver & layout
Dead-Time	The value of 15.4 ns is too narrow in implementation; 70 ns (1kΩ, 100pF) optimal at 666.66 kHz	Dead-time should be adjusted to the frequency and characteristics of the components
GaN MOSFET	All MOSFETs are damaged (short) due to spikes and cross-conduction	Requires active protection (snubber, TVS) and proper gate resistors
Full-Bridge Inverter	The box output appears at 666.66 kHz but still rings, deteriorating when the VIN is raised	The layout needs optimization to dampen ringing and maintain switching stability
Filter Band-Pass	Works well when test loose; amplitude drops when connected to the inverter	Need impedance alignment and inverter input improvements for the filter to work optimally

The fishbone diagram analysis in Figure 23 identifies six main causes of the performance differences:

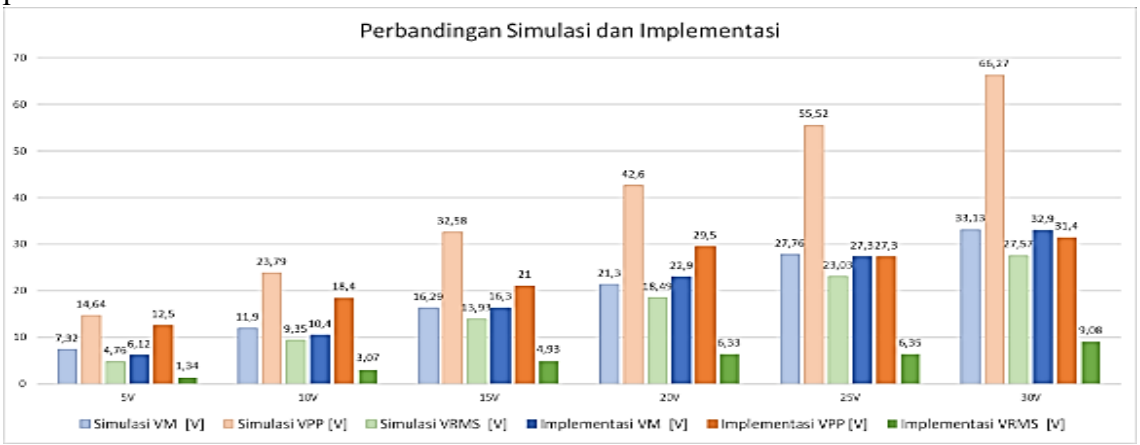


Figure 23. Simulation and Implementation Comparison Graph

Parasitic PCB layout: long switching lines and inductive loops cause ringing and overshoot.

Gate driver UCC27524: not fast enough for GaN FET, causing distortion of the gate signal. Lack of circuit protection: no snubber, TVS, or gate resistor is optimal. PWM instability: inaccurate signal at high frequencies. Poor filter integration: the inverter output is too noisy for optimal filter efficiency. MOSFET damage: due to a poor combination of dead-time, layout, and lack of protection.

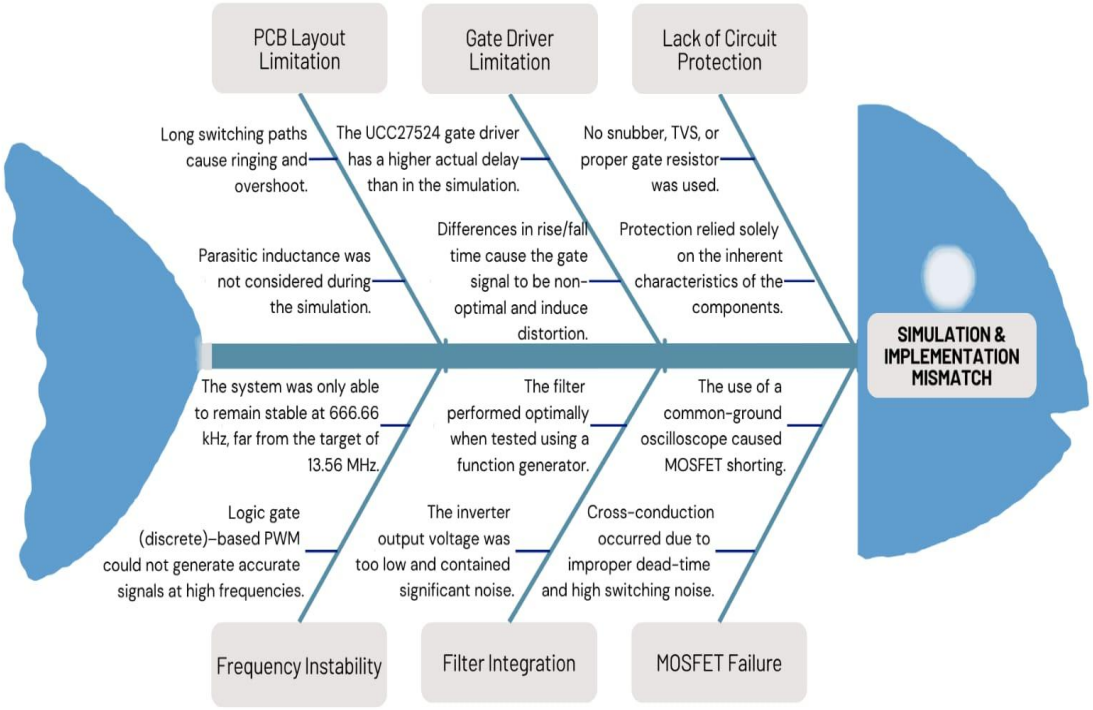


Figure 24. Fishbone Simulation & Implementation Results Diagram

CONCLUSIONS AND SUGGESTIONS

Conclusion

This research successfully designed and tested a GaN MOSFET-based full-bridge inverter for Wireless Power Transfer (WPT) applications in electric vehicle charging. The simulation results showed excellent performance at the ISM frequency of 13.56 MHz, with waves approaching sinusoidal, THD < 1%, and average power reaching ±2.13 kW at a load of 50 Ω. This proves that theoretically, the design of GaN MOSFET-based inverters is able to meet the needs of high-power WPT systems.

The physical implementation of the prototype showed significant limitations compared to the simulation. The prototype is only able to operate stably at a frequency of 666.66 kHz with a clean box waveform, but it is far from the target of 13.56 MHz. This difference is due to parasitic factors in the PCB layout, the limitation of UCC27524 drivers, and the absence of switching protections such as snubbers and TVS. The impact of this limitation can be seen in the reduction of RMS voltage to only 32.9% of the simulation results.

Overall, this research makes an important contribution to the development of WPT technology for electric vehicles, particularly in the military sector that requires high flexibility and reliability. Although the frequency target has not yet been achieved, this study proves the feasibility of the GaN MOSFET-based inverter concept and identifies critical areas that need to be optimized, such as PCB design, circuit protection, and high-speed driver selection.

Suggestion

To achieve optimal performance at the 13.56 MHz frequency, it is recommended to use a precision signal source such as a crystal-based generator or Direct Digital

Synthesizer (DDS). This will improve the frequency stability and accuracy of dead-time settings, thereby reducing the risk of cross-conduction and ringing in PWM signals.

In terms of hardware, the selection of gate drivers equipped with protection features such as UVLO and active Miller clamps is highly recommended. In addition, it is necessary to optimize the PCB layout with a multilayer configuration to minimize switching path length and parasitic inductance. The addition of a calibrated RC snubber is also important to reduce overshoot and maintain signal integrity.

For testing and system integration, it is recommended to use safe measurement techniques, such as oscilloscopes with floating grounds, to avoid the risk of inter-ground shorts. In addition, it is necessary to develop filters with impedance adjustments so that they can work optimally at high frequencies. Advanced research can also explore closed-loop controls to improve overall system stability and efficiency.

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